IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A semiconductor device comprising:

an amplifying transistor;

a biasing transistor;

an amplifying side power source line;

a biasing side power source line;

a bias signal line;

an electric discharging transistor; and

an electric discharging power source line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor, a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, and a source terminal of the amplifying transistor serves as an output terminal,

wherein one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor, and

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

2. (Previously presented) A device according to claim 1 further comprising a load capacitance wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

3. (Previously presented) A device according to claim 1, wherein the electric discharging power source line is connected to the biasing side power source line.

4-7. (Canceled)

8. (Previously presented) A device according to claim 1, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistors is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

9. (Previously presented) A device according to claim 1, wherein the amplifying transistor, the biasing transistor, and the electric discharging transistor are transistors having the same polarity.

10. (Previously presented) A scanner, which uses the semiconductor device according to claim 1.

11. (Previously presented) A digital still camera, which uses the semiconductor device according to claim 1.

12. (Previously presented) An X-ray camera, which uses the semiconductor device according to claim 1.

13. (Previously presented) A portable information terminal, which uses the semiconductor device according to claim 1.

14. (Previously presented) A computer, which uses the semiconductor device according to claim 1.

15-34. (Canceled)

35. (Previously presented) A driving method of a semiconductor device having an amplifying transistor, a biasing transistor, an amplifying side power source line, a biasing side power source line, and a bias signal line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor,

wherein a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, and a source terminal of the amplifying transistor serves as an output terminal,

wherein the driving method outputs a signal after performing a pre-discharge, and

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

36. (Previously presented) A method according to claim 35 further comprising a load capacitance wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

37-40. (Canceled)

41. (Previously presented) A method according to claim 35, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

42-56. (Canceled).

57. (Previously presented) A driving method of a semiconductor device having an amplifying

transistor, a biasing transistor, an amplifying side power source line, a biasing side power source line, and a bias signal line, an electric discharging transistor, and an electric discharging power source line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor, a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, a source terminal of the amplifying transistor serves as an output terminal, one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor,

wherein the driving method outputs a signal after performing a pre-discharge by making the electric discharging transistor into a conductive state, and

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

58. (Previously presented) A method according to claim 57, wherein a value of an electric potential of the electric discharging power source line takes a value that is between an electric potential of the bias signal line and an electric potential of the biasing side power source line.

59-70. (Canceled)

71. (New) A semiconductor device comprising:

an amplifying transistor using a first crystalline silicon film as the active layer ;

a biasing transistor using a second crystalline silicon film as the active layer;

an amplifying side power source line;

a biasing side power source line;

a bias signal line;

an electric discharging transistor using a third crystalline silicon film as the active layer; and

an electric discharging power source line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor, a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, and a source terminal of the amplifying transistor serves as an output terminal, and

wherein one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor.

72. (New) A device according to claim 71,

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

73. (New) A device according to claim 71, further comprising a load capacitance wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

74. (New) A device according to claim 71, wherein the electric discharging power source line is connected to the biasing side power source line.

75. (New) A device according to claim 71, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistors is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

76. (New) A device according to claim 71, wherein the amplifying transistor, the biasing transistor, and the electric discharging transistor are transistors having the same polarity.

77. (New) A device according to claim 71, wherein the semiconductor device is a scanner.

78. (New) A device according to claim 71, wherein the semiconductor device is a digital still camera.

79. (New) A device according to claim 71, wherein the semiconductor device is an X-ray camera.

80. (New) A device according to claim 71, wherein the semiconductor device is a portable information terminal.

81. (New) A driving method of a semiconductor device having an amplifying transistor using a first crystalline silicon film as the active layer, a biasing transistor using a second crystalline silicon film as the active layer, an amplifying side power source line, a biasing side power source line, and a bias signal line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor,

wherein a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, and a source terminal of the amplifying transistor serves as an output terminal, and

wherein the driving method outputs a signal after performing a pre-discharge.

82. (New) A method according to claim 81,

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state

83. (New) A method according to claim 81 further comprising a load capacitance wherein one terminal of the load capacitance is connected to the output terminal, and the other terminal of the load capacitance is connected to a load capacitance power source line.

84. (New) A method according to claim 81, wherein when the semiconductor device has a plurality of biasing transistors, an absolute value of a voltage between a gate and a source of the plurality of biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the entire plurality of biasing transistors into a conductive state.

85. (New) A driving method of a semiconductor device having an amplifying transistor using a first crystalline silicon film as the active layer, a biasing transistor using a second crystalline silicon film as the active layer, an amplifying side power source line, a biasing side power source line, and a bias signal line, an electric discharging transistor using a third crystalline silicon film as the active layer, and an electric discharging power source line,

wherein a drain terminal of the amplifying transistor is connected to the amplifying side power source line, a source terminal of the biasing transistor is connected to the biasing side power source line, a source terminal of the amplifying transistor is connected to a drain terminal of the biasing transistor, a gate terminal of the biasing transistor is connected to the bias signal line, a gate terminal of the amplifying transistor serves as an input terminal, a source terminal of the amplifying transistor serves as an output terminal, one of the output terminal and the electric discharging power source line is connected to a source terminal of the electric discharging transistor while the other thereof is connected to a drain terminal of the electric discharging transistor, and

wherein the driving method outputs a signal after performing a pre-discharge by making the electric discharging transistor into a conductive state.

86 (New). A method according to claim 85,

wherein an absolute value of a voltage between a gate and a source of the biasing transistor is equivalent to a minimum value of an absolute value of a voltage between a gate and a source that is necessary for making the biasing transistor into a conductive state.

87. (New) A method according to claim 85, wherein a value of an electric potential of the electric discharging power source line takes a value that is between an electric potential of the bias signal line and an electric potential of the biasing side power source line.

88. (New) A method according to claims 85, wherein the amplifying transistor, the biasing transistor, and the electric discharging transistor are transistors having the same polarity.